Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. 1OE**
2. **1A0**
3. **2Y3**
4. **1A1**
5. **2Y2**
6. **1A2**
7. **2Y1**
8. **1A3**
9. **2Y0**
10. **GND**
11. **GND**
12. **2A0**
13. **1Y3**
14. **2A1**
15. **1Y2**
16. **2A2**
17. **1Y1**
18. **2A3**
19. **1Y0**
20. **N. 2OE**
21. **VCC**
22. **VCC**

**.069”**

**14**

**13**

**12**

**11**

**10**

**9**

**8**

**19 18 17 16 15**

**20**

**21**

**22**

**1**

**2**

**3 4 5 6 7**

**MASK**

**REF**

**ACT244**

**.067”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: ACT244**

**APPROVED BY: DK DIE SIZE .067” X .069” DATE: 10/4/22**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ACT244**

**DG 10.1.2**

#### Rev B, 7/1